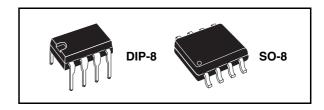


## High-voltage high and low side driver

#### **Features**

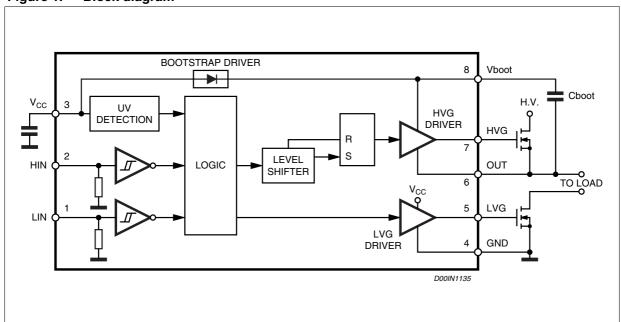
- High voltage rail up to 600 V
- dV/dt immunity ±50 V/nsec in full temperature range
- Driver current capability:
  - 400 mA source,
  - 650 mA sink
- Switching times 50/30 nsec rise/fall with 1nF load
- CMOS/TTL Schmitt trigger inputs with hysteresis and pull down
- Internal bootstrap diode
- Outputs in phase with inputs
- Interlocking function



#### **Description**

The L6387E is an high-voltage device, manufactured with the BCD"OFF-LINE" technology. It has a Driver structure that enables to drive independent referenced N Channel Power MOS or IGBT. The high side (Floating) Section is enabled to work with voltage Rail up to 600V. The Logic Inputs are CMOS/TTL compatible for ease of interfacing with controlling devices.

Figure 1. Block diagram



Contents L6387E

# **Contents**

1	Electrical data
	1.1 Absolute maximum ratings
	1.2 Thermal data
	1.3 Recommended operating conditions
2	Pin connection
3	Electrical characteristics
	3.1 AC operation
	3.2 DC operation
4	Input logic
5	Bootstrap driver
	5.1 C <sub>BOOT</sub> selection and charging
6	Typical characteristic
7	Package mechanical data1
8	Order codes
۵	Pavision history

L6387E Electrical data

### 1 Electrical data

#### 1.1 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V <sub>out</sub>	Output voltage	-3 to V <sub>boot</sub> -18	V
V <sub>cc</sub>	Supply voltage	- 0.3 to +18	V
V <sub>boot</sub>	Floating supply voltage	-1 to 618	V
$V_{hvg}$	High side gate output voltage	-1 to V <sub>boot</sub>	V
$V_{lvg}$	Low side gate output voltage	-0.3 to V <sub>cc</sub> +0.3	V
$V_{i}$	Logic input voltage	-0.3 to V <sub>cc</sub> +0.3	V
dV <sub>out</sub> /d <sub>t</sub>	Allowed output slew rate	50	V/ns
P <sub>tot</sub>	Total power dissipation (T <sub>J</sub> = 85 °C)	750	mW
T <sub>j</sub>	Junction temperature	150	°C
T <sub>s</sub>	Storage temperature	-50 to 150	°C

Note: ESD immunity for pins 6, 7 and 8 is guaranteed up to 900 V (Human Body Model)

#### 1.2 Thermal data

Table 2. Thermal data

Symbol	Parameter	SO-8	DIP-8	Unit
R <sub>th(JA)</sub>	Thermal Resistance Junction to ambient	150	100	°C/W

### 1.3 Recommended operating conditions

Table 3. Recommended operating conditions

Symbol	Pin	Parameter	Test condition	Min	Тур	Max	Unit
V <sub>out</sub>	6	Output voltage		(1)		580	V
V <sub>BS</sub> (2)	8	Floating supply voltage		(1)		17	V
f <sub>sw</sub>		Switching frequency	HVG,LVG load C <sub>L</sub> = 1nF			400	kHz
V <sub>cc</sub>	3	Supply voltage				17	٧
T <sub>J</sub>		Junction temperature		-45		125	°C

<sup>1.</sup> If the condition Vboot - Vout < 18V is guaranteed, Vout can range from -3 to 580V

577

<sup>2.</sup>  $V_{BS} = V_{boot} - V_{out}$ 

Pin connection L6387E

# 2 Pin connection

Figure 2. Pin connection (Top view)

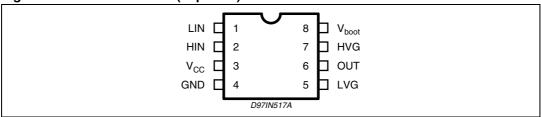


Table 4. Pin description

N°	Pin	Туре	Function			
1	LIN	I	Low side driver logic input			
2	HIN	I	High side driver logic input			
3	V <sub>cc</sub>		Low voltage power supply			
4	GND		Ground			
5	LVG (1)	0	Low side driver output			
6	VOUT	0	High side driver floating reference			
7	HVG (1)	0	High side driver output			
8	V <sub>boot</sub>		Bootstrap supply voltage			

<sup>1.</sup> The circuit guarantees 0.3V maximum on the pin (@ Isink = 10mA). This allows to omit the "bleeder" resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low.

# 3 Electrical characteristics

## 3.1 AC operation

Table 5. AC operation electrical characteristcs  $(V_{CC} = 15V; T_J = 25^{\circ}C)$ 

Symbol	Pin	Parameter	Test condition	Min	Тур	Max	Unit
t <sub>on</sub>		High/low side driver turn-on propagation delay	V <sub>out</sub> = 0V		110		ns
t <sub>off</sub>	1 vs 5 2 vs 7	High/low side driver turn-off propagation delay	V <sub>out</sub> = 0V		105		ns
t <sub>r</sub>	5, 7	Rise time	C <sub>L</sub> = 1000pF		50		ns
t <sub>f</sub>	5, 7	Fall time	C <sub>L</sub> = 1000pF		30		ns

## 3.2 DC operation

Table 6. DC operation electrical characteristcs  $(V_{CC} = 15V; T_J = 25^{\circ}C)$ 

Pin	Parameter	Test condition	Min	Тур	Max	Unit			
∟ow supply voltage section									
	Supply voltage				17	V			
	V <sub>cc</sub> UV turn on threshold		5.5	6	6.5	V			
	V <sub>cc</sub> UV turn off threshold		5	5.5	6	V			
	V <sub>cc</sub> UV hysteresis			0.5		V			
3	Undervoltage quiescent supply current	V <sub>cc</sub> ≤5V		150	220	μΑ			
	Quiescent current	V <sub>cc</sub> = 15V		250	320	μΑ			
	Bootstrap driver on resistance <sup>(1)</sup>	V <sub>cc</sub> ≥ 12.5V		125		Ω			
pped	supply voltage section								
	Bootstrap supply voltage				17	V			
8	V <sub>BS</sub> quiescent current	HVG ON			100	μΑ			
	High voltage leakage current	$V_{hvg} = V_{out} = V_{boot} = 600V$			10	μА			
side	driver								
E 7	Source short circuit current	$V_{IN} = V_{ih} (tp < 10 \mu s)$	300	400		mA			
5,7	Sink short circuit current	$V_{IN} = V_{il} (tp < 10\mu s)$	450	650		mA			
	3 pped:	Supply voltage  V <sub>cc</sub> UV turn on threshold  V <sub>cc</sub> UV turn off threshold  V <sub>cc</sub> UV hysteresis  Undervoltage quiescent supply current  Quiescent current  Bootstrap driver on resistance(1)  pped supply voltage section  Bootstrap supply voltage  V <sub>BS</sub> quiescent current  High voltage leakage current  side driver  Source short circuit current	Supply voltage  V <sub>cc</sub> UV turn on threshold  V <sub>cc</sub> UV turn off threshold  V <sub>cc</sub> UV hysteresis  Undervoltage quiescent supply current  Quiescent current  Bootstrap driver on resistance(1)  Pred supply voltage section  Bootstrap supply voltage  V <sub>cc</sub> $\geq 12.5$ V  Pred supply voltage section  Bootstrap supply voltage  V <sub>BS</sub> quiescent current  HVG ON  High voltage leakage current  V <sub>IN</sub> = V <sub>out</sub> = V <sub>out</sub> = V <sub>boot</sub> = 600V  Side driver  Source short circuit current  V <sub>IN</sub> = V <sub>ih</sub> (tp < 10µs)	Supply voltage  V <sub>cc</sub> UV turn on threshold  V <sub>cc</sub> UV turn off threshold  V <sub>cc</sub> UV hysteresis  Undervoltage quiescent supply current  Quiescent current  Bootstrap driver on resistance <sup>(1)</sup> V <sub>cc</sub> $\geq$ 12.5V  Pped supply voltage section  Bootstrap supply voltage  V <sub>BS</sub> quiescent current  High voltage leakage current  V <sub>IN</sub> = V <sub>out</sub> = V <sub>out</sub> = V <sub>boot</sub> = 600V  Side driver  Source short circuit current  V <sub>IN</sub> = V <sub>ih</sub> (tp < 10µs)  300	Supply voltage   Supply voltage   V <sub>cc</sub> UV turn on threshold   5.5   6   V <sub>cc</sub> UV turn off threshold   5   5.5     V <sub>cc</sub> UV turn off threshold   5   5.5     Undervoltage quiescent supply current   V <sub>cc</sub> $\leq$ 5V   150   Rootstrap driver on resistance(1)   V <sub>cc</sub> $\geq$ 12.5V   125   Piped supply voltage section   Souther Supply voltage   V <sub>BS</sub> quiescent current   HVG ON   High voltage leakage current   V <sub>hvg</sub> = V <sub>out</sub> = V <sub>boot</sub> = 600V   Side driver   Source short circuit current   V <sub>IN</sub> = V <sub>ih</sub> (tp < 10µs)   300   400   400   Side driver   V <sub>IN</sub> = V <sub>ih</sub> (tp < 10µs)   300   400   V <sub>IN</sub> = V <sub>ih</sub> (tp < 10µs)   300   400   V <sub>IN</sub> = V <sub>ih</sub> (tp < 10µs)   300   400   V <sub>IN</sub> = V <sub>ih</sub> (tp < 10µs)   300   400   V <sub>IN</sub> = V <sub>ih</sub> (tp < 10µs)   300   400   V <sub>IN</sub> = V <sub>ih</sub> (tp < 10µs)   300   400   V <sub>IN</sub> = V <sub>ih</sub> (tp < 10µs)   300   400   V <sub>IN</sub> = V <sub>ih</sub> (tp < 10µs)   300   400   V <sub>IN</sub> = V <sub>ih</sub> (tp < 10µs)   300   400   V <sub>IN</sub> = V <sub>ih</sub> (tp < 10µs)   300   400   V <sub>IN</sub> = V <sub>ih</sub> (tp < 10µs)   300   400   V <sub>IN</sub> = V <sub>ih</sub> (tp < 10µs)   300   400   V <sub>IN</sub> = V <sub>ih</sub> (tp < 10µs)   300   400   V <sub>IN</sub> = V <sub>ih</sub> (tp < 10µs)   300   400   V <sub>IN</sub> = V <sub>ih</sub> (tp < 10µs)   300   400   V <sub>IN</sub> = V <sub>ih</sub> (tp < 10µs)   300   400   V <sub>IN</sub> = V <sub>ih</sub> (tp < 10µs)   300   400   V <sub>IN</sub> = V <sub>ih</sub> (tp < 10µs)   300   400   V <sub>IN</sub> = V <sub>ih</sub> (tp < 10µs)   300   400   V <sub>IN</sub> = V <sub>ih</sub> (tp < 10µs)   300   400   V <sub>IN</sub> = V <sub>ih</sub> (tp < 10µs)   300   400   V <sub>IN</sub> = V <sub>ih</sub> (tp < 10µs)   300   400   V <sub>IN</sub> = V <sub>IN</sub>   300   400   V <sub>IN</sub> = V <sub>IN</sub>   300   400   400   V <sub>IN</sub>   300   400   V <sub></sub>	poly voltage section  Supply voltage   17 $V_{cc}$ UV turn on threshold   5.5   6   6.5 $V_{cc}$ UV turn off threshold   5   5.5   6 $V_{cc}$ UV hysteresis   0.5  Undervoltage quiescent supply current   $V_{cc} \le 5V$   150   220  Quiescent current   $V_{cc} = 15V$   250   320  Bootstrap driver on resistance(1)   $V_{cc} \ge 12.5V$   125  poped supply voltage section  Bootstrap supply voltage   17 $V_{BS}$ quiescent current   HVG ON   100  High voltage leakage current   $V_{hvg} = V_{out} = V_{boot} = 600V$   10  side driver  Source short circuit current   $V_{IN} = V_{ih}$ (tp < 10 $\mu$ s)   300   400			

5/15

Input logic L6387E

Table 6: De operation electrical orial action (continued) (VCC = 10 V, 1j = 20								
Symbol	Pin	Parameter	Test condition	Min	Тур	Max	Unit	
Logic inp	outs							
V <sub>il</sub>		Low level logic threshold voltage				1.5	V	
V <sub>ih</sub>	1,2	High level logic threshold voltage		3.6			V	
l <sub>ih</sub>		High level logic input current	V <sub>IN</sub> = 15V		50	70	μA	
l <sub>il</sub>		Low level logic input current	$V_{INI} = 0V$			1	μA	

Table 6. DC operation electrical characteristcs (continued)( $V_{CC} = 15V$ ;  $T_J = 25$ °C)

$$\mathsf{R}_{\mathsf{DSON}} = \frac{(\mathsf{V}_{\mathsf{CC}} - \mathsf{V}_{\mathsf{CBOOT1}}) - (\mathsf{V}_{\mathsf{CC}} - \mathsf{V}_{\mathsf{CBOOT2}})}{\mathsf{I}_1(\mathsf{V}_{\mathsf{CC}}, \mathsf{V}_{\mathsf{CBOOT1}}) - \mathsf{I}_2(\mathsf{V}_{\mathsf{CC}}, \mathsf{V}_{\mathsf{CBOOT2}})}$$

where  $I_1$  is pin 8 current when  $V_{CBOOT} = V_{CBOOT1}$ ,  $I_2$  when  $V_{CBOOT} = V_{CBOOT2}$ 

## 4 Input logic

L6387E Input Logic is  $V_{CC}$  (17V) compatible. An interlocking features is offered (see truth table below) to avoid undesired simultaneous turn ON of both Power Switches driven.

Table 7. Input logic

Input	HIN	0	0	1	1
Input	LIN	0	1	0	1
0.44	HVG	0	0	1	0
Output	LVG	0	1	0	0

<sup>1.</sup>  $R_{DS(on)}$  is tested in the following way:

L6387E Bootstrap driver

### 5 Bootstrap driver

A bootstrap circuitry is needed to supply the high voltage section. This function is normally accomplished by a high voltage fast recovery diode (*Figure 3* a). In the L6387E a patented integrated structure replaces the external diode. It is realized by a high voltage DMOS, driven synchronously with the low side driver (LVG), with in series a diode, as shown in *Figure 3* b. An internal charge pump (*Figure 3* b) provides the DMOS driving voltage. The diode connected in series to the DMOS has been added to avoid undesirable turn on of it.

#### 5.1 C<sub>BOOT</sub> selection and charging

To choose the proper  $C_{BOOT}$  value the external MOS can be seen as an equivalent capacitor. This capacitor  $C_{EXT}$  is related to the MOS total gate charge:

$$C_{EXT} = \frac{Q_{gate}}{V_{gate}}$$

The ratio between the capacitors  $C_{\text{EXT}}$  and  $C_{\text{BOOT}}$  is proportional to the cyclical voltage loss. It has to be:

e.g.: if  $Q_{gate}$  is 30nC and  $V_{gate}$  is 10V,  $C_{EXT}$  is 3nF. With  $C_{BOOT}$  = 100nF the drop would be 300mV.

If HVG has to be supplied for a long time, the  $C_{BOOT}$  selection has to take into account also the leakage losses.

e.g.: HVG steady state consumption is lower than 200 $\mu$ A, so if HVG T<sub>ON</sub> is 5ms, C<sub>BOOT</sub> has to supply 1 $\mu$ C to C<sub>EXT</sub>. This charge on a 1 $\mu$ F capacitor means a voltage drop of 1V.

The internal bootstrap driver gives great advantages: the external fast recovery diode can be avoided (it usually has great leakage current).

This structure can work only if  $V_{OUT}$  is close to GND (or lower) and in the meanwhile the LVG is on. The charging time ( $T_{charge}$ ) of the  $C_{BOOT}$  is the time in which both conditions are fulfilled and it has to be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the DMOS  $R_{DSON}$  (typical value: 125  $\Omega$ ). At low frequency this drop can be neglected. Anyway increasing the frequency it must be taken in to account.

The following equation is useful to compute the drop on the bootstrap DMOS:

$$V_{drop} = I_{charge}R_{dson} \rightarrow V_{drop} = \frac{Q_{gate}}{T_{charge}}R_{dson}$$

where  $Q_{gate}$  is the gate charge of the external power MOS,  $R_{dson}$  is the on resistance of the bootstrap DMOS, and  $T_{charge}$  is the charging time of the bootstrap capacitor.

577

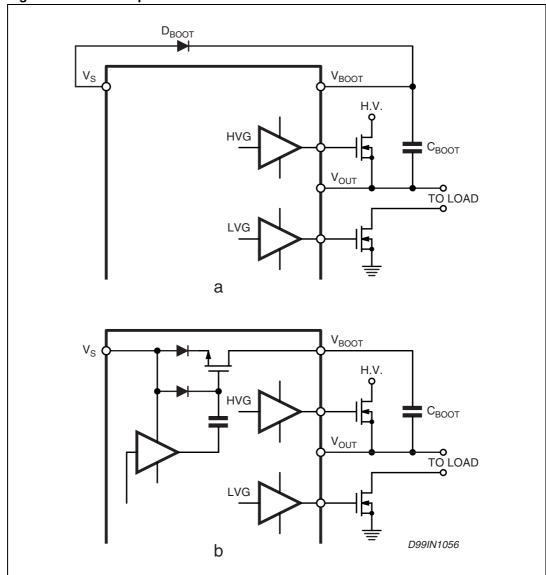
Bootstrap driver L6387E

For example: using a power MOS with a total gate charge of 30nC the drop on the bootstrap DMOS is about 1V, if the  $T_{charge}$  is  $5\mu s$ . In fact:

$$V_{drop} = \frac{30nC}{5\mu s} \cdot 125\Omega \sim 0.8V$$

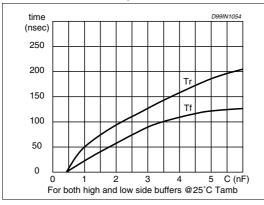
 $V_{drop}$  has to be taken into account when the voltage drop on  $C_{BOOT}$  is calculated: if this drop is too high, or the circuit topology doesn't allow a sufficient charging time, an external diode can be used.

Figure 3. Bootstrap driver



# 6 Typical characteristic

Figure 4. Typical rise and fall times vs Figure 5. Quiescent current vs supply load capacitance voltage



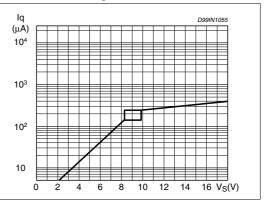
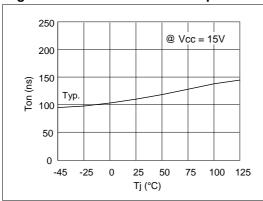


Figure 6. Turn on time vs temperature Figure 7. Turn Off time vs temperature



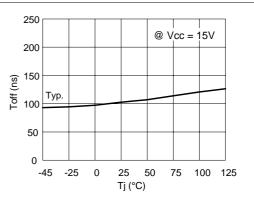


Figure 8. Output source current vs temperature

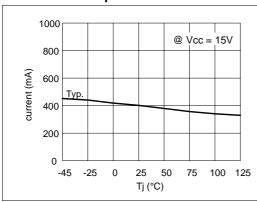
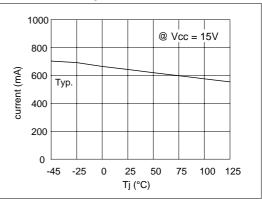


Figure 9. Output sink current vs temperature



## 7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Figure 10. DIP-8 mechanical data and package dimensions

DIM.		mm			inch		OUTLINE AND	
/IIVI.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	OUTLINE AND MECHANICAL DATA	
Α		3.32			0.131			
a1	0.51			0.020				
В	1.15		1.65	0.045		0.065		
b	0.356		0.55	0.014		0.022		
b1	0.204		0.304	0.008		0.012		
D			10.92			0.430		
Е	7.95		9.75	0.313		0.384		
е		2.54			0.100		ų ·	
еЗ		7.62			0.300			
e4		7.62			0.300			
F			6.6			0.260		
I			5.08			0.200		
L	3.18		3.81	0.125		0.150	DIP-8	
Z			1.52			0.060		
e4  B B1  E  Z								
			8	D	5			

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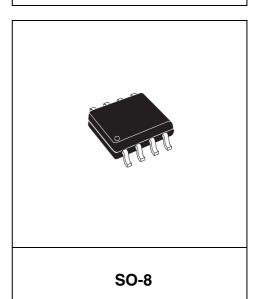
Figure 11. SO-8 mechanical data and package dimensions

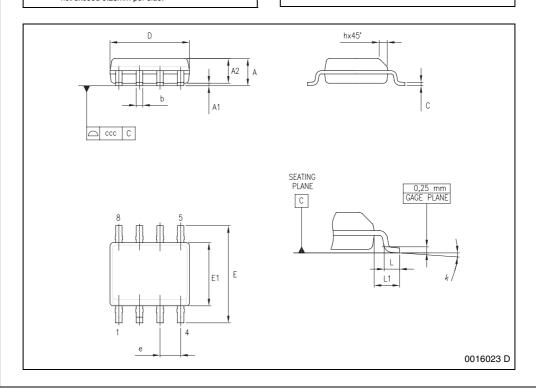
DIM.		mm		inch			
DIW.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Α			1.750			0.0689	
A1	0.100		0.250	0.0039		0.0098	
A2	1.250			0.0492			
b	0.280		0.480	0.0110		0.0189	
С	0.170		0.230	0.0067		0.0091	
D (1)	4.800	4.900	5.000	0.1890	0.1929	0.1969	
Е	5.800	6.000	6.200	0.2283	0.2362	0.2441	
E1 <sup>(2)</sup>	3.800	3.900	4.000	0.1496	0.1535	0.1575	
е		1.270			0.0500		
h	0.250		0.500	0.0098		0.0197	
L	0.400		1.270	0.0157		0.0500	
L1		1.040			0.0409		
k	0°		8°	0°		8°	
ccc			0.100			0.0039	

Notes: 1. Dimensions D does not include mold flash,

Dimensions D does not include mold flash, profrusions or gate burrs.
 Mold flash, potrusions or gate burrs shall not exceed 0.15mm in total (both side).
 Dimension "E1" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

#### **OUTLINE AND MECHANICAL DATA**





L6387E Order codes

# 8 Order codes

Table 8. Order codes

Part number	Package	Packaging
L6387E	DIP-8	Tube
L6387ED	SO-8	Tube
L6387ED013TR	SO-8	Tape and reel

Revision history L6387E

# 9 Revision history

Table 9. Document revision history

Date	Revision	Changes
11-Oct-2007	1	First release
19-Sep-2008	2	Minor text changes on Table 6

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